WHAT IS CLAIMED IS:

1. A method of forming a power semiconductor device comprising the steps of:

A. providing a substrate of a first or second conductivity type;

B. forming a voltage sustaining region on said substrate by:

1. depositing an epitaxial layer on the substrate, said epitaxial layer having a first conductivity type;

2. etching at least one trench in the epitaxial layer with an etchant gas having a dopant species of the second conductivity type to form a doped surface layer in a portion of the epitaxial layer defining the trench walls;

3. diffusing further into the epitaxial layer the dopant species located in said doped surface layer to form a doped epitaxial region adjacent to the trench and in the epitaxial layer;

4. depositing a filler material in said trench to substantially fill said trench; and

C. forming over said voltage sustaining region at least one region of said second conductivity type to define a junction therebetween.

2. The method of claim 1 wherein the step of depositing the filler material is performed before the step of diffusing the dopant species.

3. The method of claim 1 wherein the step of depositing the filler material is performed after the step of diffusing the dopant species.

4. The method of claim 1 wherein step (C) further includes the steps of:

forming a gate conductor above a gate dielectric region;

forming first and second body regions in the epitaxial layer to define a drift region therebetween, said body regions having a second conductivity type;

forming first and second source regions of the first conductivity type in the first and second body regions, respectively.

5. The method of claim 1 wherein said material filling the trench is undoped polysilicon.

6. The method of claim 1 wherein said material filling the trench is a dielectric material.

7. The method of claim 6 wherein said dielectric material is silicon dioxide.

8. The method of claim 6 wherein said dielectric material is silicon nitride.

9. The method of claim 1 wherein said dopant species is boron.

10. The method of claim 9 wherein said etchant gas is BCl_3.

11. The method of claim 1 wherein said dopant species is phosphorus.

12. The method of claim 11 wherein said etchant gas is PH_3.

13. The method of claim 4 wherein said body regions include deep body regions.

14. The method of claim 1, wherein said trench is formed by providing a masking layer defining at least one trench, and etching the trench defined by the masking layer.

15. The method of claim 1 wherein the etching step is performed by reactive ion etching.

16. The method of claim 4, wherein said body region is formed by implanting and diffusing a dopant into the substrate.

17. The method of claim 1 wherein said power semiconductor device is selected from the group consisting of a vertical DMOS, V-groove DMOS, and a trench DMOS MOSFET, an IGBT, and a bipolar transistor.

18. A power semiconductor device made in accordance with the method of claim 1.

19. A power semiconductor device made in accordance with the method of claim 4.

20. A power semiconductor device made in accordance with the method of claim 17.

21. A power semiconductor device comprising:

a substrate of a first or second conductivity type;

a voltage sustaining region disposed on said substrate, said voltage sustaining region including:

an epitaxial layer having a first conductivity type;

at least one trench located in said epitaxial layer;

at least one doped column having a dopant of a second conductivity type, said column being formed from a dopant introduced into surfaces of the trench by an etchant gas used to form the trench and which is diffused into the epitaxial layer;

a filler material substantially filling said trench; and

at least one region of said second conductivity disposed over said voltage sustaining region to define a junction therebetween.

22. The device of claim 21 wherein said at least one region further includes:

a gate dielectric and a gate conductor disposed above said gate dielectric;

first and second body regions located in the epitaxial layer to define a drift region therebetween, said body regions having a second conductivity type; and

first and second source regions of the first conductivity type located in the first and second body regions, respectively.

23. The device of claim 21 wherein said material filling the trench is undoped polysilicon.

24. The device of claim 21 wherein said material filling the trench is a dielectric material.

25. The device of claim 24 wherein said dielectric material is silicon dioxide.

26. The device of claim 24 wherein said dielectric material is silicon nitride.

27. The device of claim 21 wherein said dopant is boron.

28. The device of claim 27 wherein said etchant gas is BCl3.

29. The device of claim 21 wherein said dopant is phosphorus.

30. The device of claim29 wherein said etchant gas is PH3.

31. The device of claim 22 wherein said body regions include deep body regions.

32. The device of claim 21 wherein said power semiconductor device is selected from the group consisting of a vertical DMOS, V-groove DMOS, and a trench DMOS MOSFET, an IGBT, and a bipolar transistor.